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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,948	07/03/2003	Hisashi Ishikawa	00862.023127.	5415

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
VO, QUANG N	
ART UNIT	**PAPER NUMBER**
2625	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,948	ISHIKAWA, HISASHI	
	Examiner	Art Unit	
	Quang N. Vo	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) *8-19, 27-38, 40-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,20-26 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 8-19, 27-38, 40-61 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 6/15/2007.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 39 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 39 is drawn to functional descriptive material NOT claimed as residing on a computer readable medium. MPEP 2106.IV.B.1 (a) (Functional Descriptive Material) states:

"Data structures not claimed as embodied in a computer-readable medium are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer."

"Such claimed data structures do not define any structural or functional interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized."

Claim 39, while defining a program, does not define a "computer-readable medium" and is thus non-statutory for that reasons. A program can range from paper on which the program is written, to a program simply contemplated and memorized by a

person. The examiner suggests amending the claim to embody the program on "computer-readable medium" in order to make the claim statutory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 20-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (Nakano) (US 6,977,756) in view of Ishikawa (US 6,956,674).

With regard to claim 1, Nakano discloses an image processing apparatus comprising: a quantization component that quantizes input image data (e.g., error diffusion, column 5, lines 24-27); a calculation component that calculates a quantization error generated by quantization by said quantization component (e.g., an error diffusion computing unit, column 5, lines 29-30); a buffer that stores the calculated quantization error (e.g., error holding register, column 5, lines 31-35); an error diffusion component that diffuses the quantization error on the basis of at least a quantization error of a first pixel, which is stored in said buffer, and a quantization error of a second pixel, which is calculated by said calculation component (e.g., the error diffusion computing unit, column 5, lines 29-40; column 10, lines 6-10).

Nakano differs from claim 1, in that he does not explicitly teach reduction component that reduces the impact of an arithmetic error by said error diffusion component on a next input image data.

Ishikawa discloses reduction component that reduces the impact of an arithmetic error by said error diffusion component on a next input image data (e.g., the multivalued dithering part 7, column 3, lines 51-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano to include reduction component that reduces the impact of an arithmetic error by said error diffusion component on a next input image data as taught by Ishikawa. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano by the teaching of Ishikawa to increase processing speed and to reduce computing (arithmetic) error in error diffusion (column 4, lines 26-31).

With regard to claim 2, Ishikawa discloses wherein said reduction component includes a connecting component that connects a decimal portion of a correction value generated by said error diffusion component to diffuse the quantization error to a lower bit side of the next input image data (column 3, lines 56-61).

With regard to claim 3, Nakano discloses further comprising a stop component that stops propagating the correction value in a case in which it is inappropriate to propagate the correction value to next and subsequent pixels (column 5, lines 58-61).

With regard to claim 4, Nakano differs from claim 4, in that he does not teach explicitly connecting decimal portion to the lower bit side of the next input image data.

Ishikawa discloses connecting decimal portion to the lower bit side of the next input image data (column 3, lines 56-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano to include connecting decimal portion to the lower bit side of the next input image data as taught by Ishikawa. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano by the teaching of Ishikawa to increase processing speed and to reduce computing (arithmetic) error in error diffusion (column 4, lines 26-31).

With regard to claim 5, Nakano discloses further comprising a processing limit component that limits clearing by said clear component when a scanning direction of the input image is reversed (e.g., adder 9 detects forward and reversed direction, column 9, lines 13-34).

With regard to claim 6, Nakano discloses wherein the case in which it is inappropriate to propagate the correction value to next and subsequent pixels includes at least one of a case in which a pixel of interest is a start pixel of a line, a case in which the pixel of interest has a value equal to a lower limit level of the input image, and a case in which the pixel of interest has a value equal to an upper limit level of the input image (column 8, line 48 – column 9, line 3).

With regard to claim 7, Nakano discloses further comprising a numerical value limit component that limits the quantization error calculated by said calculation component to a numerical value within a predetermined range (column 11, lines 19-33).

With regard to claim 20, Nakano discloses a method for image processing comprising the steps of: quantizing input image data (e.g., error diffusion, column 5, lines 24-27); calculating a quantization error generated in said quantization step (e.g.,

an error diffusion computing unit, column 5, lines 29-30); storing the calculated quantization error in a buffer (e.g., error holding register, column 5, lines 31-35); diffusing the quantization error on the basis of at least a quantization error of a first pixel, which is stored in said buffer, and a calculated quantization error of a second pixel (e.g., the error diffusion computing unit, column 5, lines 29-40).

Nakano differs from claim 20, in that he does not explicitly teach reducing the impact of an arithmetic error due to said error diffusion step on next input image data.

Ishikawa discloses reduction component that reduces the impact of an arithmetic error by said error diffusion component on a next input image data (e.g., the multivalued dithering part 7, column 3, lines 51-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano to include reduction component that reduces the impact of an arithmetic error by said error diffusion component on a next input image data as taught by Ishikawa. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano by the teaching of Ishikawa to increase processing speed and to reduce computing (arithmetic) error in error diffusion (column 4, lines 26-31).

With regard to claim 21, Ishikawa discloses wherein said reducing step includes a step for connecting a decimal portion of a correction value generated in said error diffusion step to diffuse the quantization error to a lower bit side of the next input image data (column 3, lines 56-61).

With regard to claim 22, Nakano discloses further comprising a step for stopping propagation of the correction value in a case in which it is inappropriate to propagate the correction value to next and subsequent pixels (column 5, lines 58-61).

With regard to claim 23, Nakano differs from claim 4, in that he does not teach explicitly connecting decimal portion to the lower bit side of the next input image data.

Ishikawa discloses connecting decimal portion to the lower bit side of the next input image data (column 3, lines 56-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano to include connecting decimal portion to the lower bit side of the next input image data as taught by Ishikawa. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Nakano by the teaching of Ishikawa to increase processing speed and to reduce computing (arithmetic) error in error diffusion (column 4, lines 26-31).

With regard to claim 24, Nakano discloses further comprising a step for limiting clear process of said clear step when a scanning direction of the input image is reversed (e.g., adder 9 detects forward and reversed direction, column 9, lines 13-34).

With regard to claim 25, Nakano discloses wherein the case in which it is inappropriate to propagate the correction value to next and subsequent pixels includes at least one of a case in which a pixel of interest is a start pixel of a line, a case in which the pixel of interest has a value equal to a lower limit level of the input image, and a case in which the pixel of interest has a value equal to an upper limit level of the input image (column 8, line 48 – column 9, line 3).

With regard to claim 26, Nakano discloses further comprising a step for limiting the quantization error calculated in said calculation step to a numerical value within a predetermined range (column 11, lines 19-33).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Vo whose telephone number is 5712701121. The examiner can normally be reached on 7:30AM-5:00PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 5712727440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Quang N. Vo 7/30/07
Patent Examiner

KING Y. POON
~~PRIMARY~~ EXAMINER
Supervisory Patent